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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
RUTTEN, JAMES D	
ART UNIT	PAPER NUMBER
2192	

DATE MAILED: 04/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/773,387	SWAINE ET AL.	
	Examiner	Art Unit	
	J. Derek Rutten	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Acknowledgement is made of Applicant's response dated November 12 2004, responding to the July 16 2004 Office Action provided in the rejection of claims 1-24, wherein claims 11, 15, and 24 have been amended, no new claims have been added, and no claims have been canceled. Claims 1-24 remain pending in the application and have been fully considered by the examiner.

2. Applicant has primarily argued that the claims are not obvious over applicant's own "Description of Prior Art" section of the originally filed specification (hereinafter "DPA") in view of U.S. Patent 6681321 to Dale et al. (hereinafter "Dale") because it does not teach generating a place holder for insertion of late data into a data stream, or inserting a late data value with an identifier at a later point. This argument is not persuasive, as will be addressed under the *Response to Arguments* section below.

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Response to Arguments

4. Applicant argues on pages 9-11, particularly page 11 paragraph 2 of the response, that the Dale reference does not teach "generating a data place holder or insertion of late data into a data stream." The essence of the argument appears to be that Dale stores information regarding every instruction, and thus does not store information in response to a data miss. While Dale does not appear to expressly disclose such terms, it does describe the occasion of a required cache load in column 2 lines 7-10:

> When a **cache load is necessary to obtain** instructions that are not already stored in the instruction cache or **data that is not already stored in the data cache**, updated cache information is stored in the trace storage device.

This passage, while not expressly using the term "data miss," is effectively describing a response to a data miss since "a cache load is necessary to obtain ... data that is not already stored in the data cache." Simply, a cache load occurs in response to a data miss. The events are logically equivalent since a data miss without a responsive cache load would result in a functional error. Regardless, Dale teaches acting in response to a data miss. Dale further describes storing trace data in response to cache events in column 5 lines 22-24:

> The trace storage device 495 need not maintain the data structures and "snap shots" in real time but may do so based on discrete events.

Thus, while Dale stores information regarding every instruction, Dale teaches storing this information in response to discrete cache events. Dale's placeholders are then arranged in response to a cache event to be placed sequentially as pointed out by the applicant on page 10 of the response. This is in accordance with the language of claim 1 which recites "...responsive to

said data miss to generate a data place holder within said stream of trace data at a position where data identifying said data value would have been placed if said data miss had not occurred."

5. Applicant has attempted to distinguish the claims from the prior art by alleging that Dale's storage of information for all fetched instruction and data is contrary to what is recited in the independent claims (page 10 paragraph 2 of the response). However, the independent claims (e.g. claim 1-iii: "a tracing circuit operable to generate a stream of trace data identifying processing instructions executed and data values accessed by said processing circuit") appear to claim this very limitation. If applicant's invention is not involved in tracing the execution of instructions and access of data, then the claims should be amended and/or clarification provided.

6. Applicant essentially argues in the last paragraph on page 11 continuing on page 12 that Dale does not teach inserting a late data value with an identifier at a later point in the trace stream. Applicant appears to suggest that Dale uses an instruction stream reconstruction device to reconstruct the entire instruction stream whereas the present invention simply inserts the late data into the stream. However, as applicant has argued, Dale does in fact insert the late data into the instruction stream as recited in the claim. The broad language used in the claim does not specify any particular implementation of data insertion into the stream. Therefore, as pointed out on page 11 of the response, Dale teaches this limitation.

Claim Rejections - 35 USC § 103

7. Claims 1-4, 7, 12-17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the "Description of the Prior Art" section on pages 2 and 3 of the originally filed specification (hereinafter referred to as "DPA") in view of Dale.

As per claim 1, DPA discloses:

(i) a processing circuit operable to process data values under control of processing instructions;

(ii) a memory operable to store data values to be processed, said processing circuit being responsive to a data access instruction to access a data value stored within said memory; and

(iii) a tracing circuit operable to generate a stream of trace data identifying processing instructions executed and data values accessed by said processing circuit;

(See page 2, lines 13-15: "Tracing the **activity** of a data processing system whereby a **trace stream is generated** including **data** representing the step-by-step activity within the system is a highly useful tool in system development."; also page 2, lines 19-21: "Examples of such on-chip tracing mechanisms are the **Embedded Trace Macrocell** provided by ARM Limited, Cambridge, England in association with their **ARM7 and ARM9 processors**." ARM7 and ARM9 processors inherently process data values under control of processing instructions, otherwise they would not have any functional value. They also contain memory for data storage and inherently use access instructions for accessing the data from memory, otherwise they would not be able to process the data. The Embedded Trace Macrocell, or "ETM", is the tracing circuit that

identifies instructions and data used by the ARM chip. Note that further information regarding ARM9 processors can be found in "ARM966E-S: Technical Reference Manual" by ARM Limited.)

wherein

(iv) a data access instruction may result in a data miss such that a data value corresponding to said data access instruction is accessed upon a processing cycle subsequent to that upon which said access would occur without said data miss (page 3 lines 5-12: "However, should a **load miss** occur whereby **the load of the data value cannot be satisfied** from the cache and requires a slower non-cache access, such as to a main memory, then the **data value will not be returned for possibly many processing cycles**. Rather than halt data processing, it is known to provide systems, such as the ARM1020T processor, in which other program instructions can continue to execute whilst the data from the previous load miss is still awaited providing those later instructions do not require or depend on the data value that has not yet been retrieved.").

DPA does not disclose generating a data placeholder or insertion of late data into a data stream.

However, in an analogous environment, Dale teaches:

(v) said tracing circuit is responsive to said data miss to generate a data place holder within said stream of trace data at a position where data identifying said data value would have been placed if said data miss had not occurred; See column 2 lines 16-19:

> As instructions are scheduled, unique **identifier information** for the scheduled instructions is stored in the trace storage device in association with the address information of the instructions.

and then, when said access to said data value does occur, to insert at a later point in said stream of trace data a late data value identifying said data value; See column 2 lines 7-10:

> When a cache load is necessary to obtain instructions that are not already stored in the instruction cache or data that is not already stored in the data cache, **updated cache information** is **stored in the trace storage** device.

Also, see column 2 lines 7-10:

> When a **cache load is necessary to obtain** instructions that are not already stored in the instruction cache or **data that is not already stored in the data cache**, updated cache information is stored in the trace storage device.

Also see column 5 lines 22-24:

> The trace storage device 495 need not maintain the data structures and "snap shots" in real time but may do so **based on discrete events**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Dale's identifier information in the tracing circuit of DPA. One of ordinary skill would have been motivated to collect accurate non-disruptive execution traces of out-of-order processors in order to examine program behavior.

As per claim 2, the above rejection of claim 1 is incorporated. DPA further discloses *the apparatus as claimed in claim 1, wherein said memory comprises a cache memory and a main memory, a data miss occurring when a data value being accessed is not stored within said cache memory* (DPA page 3 lines 5-8).

As per claim 3, the above rejection of claim 1 is incorporated. DPA does not expressly disclose tag values. However, in an analogous environment, Dale teaches *said*

data place holder includes a tag value and said late data value includes a matching tag value (column 7 line 52 – column 8 line 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Dale's tags with the tracing circuit of DPA. One of ordinary skill in the art would have been motivated to correlate two pieces of data for further analysis.

As per claim 4, the above rejection of claim 3 is incorporated. DPA does not expressly disclose late data values generated in a different order than their corresponding data misses. However, Dale teaches out-of-order execution and the collection of data in a different order than the instructions issued (column 5 line 45-52).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement Dale's handling of out-of-order execution in the tracing circuit of DPA. One of ordinary skill would have been motivated to anticipate the varying latencies between different elements of a memory hierarchy to ensure the proper collection of data.

As per claim 7, DPA further discloses *the apparatus as claimed in claim 1, wherein said tracing circuit is operable to control tracing operation in response to a trigger condition associated with one or more of said data value and a memory address associated with said data value* (page 2 lines 19-21. Trigger conditions are supported by the Embedded Trace Macrocell.).

As per claim 12, DPA also/further discloses a method (page 2 lines 13-15: "step-by-step"). All other limitations have been addressed in the above rejection of claim 1.

As per claim 13, DPA discloses *controlling a data processing apparatus to analyze a stream of trace data* (as addressed in the above rejection of claim 12). DPA does not expressly disclose a computer program product. However, Dale teaches the use of a computer program product (column 11 line 37 – column 12 line 14).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Dale's computer program product with the tracing circuit of DPA. One of ordinary skill in the art would have been motivated to sell and distribute the computer program.

All other limitations have been addressed in the above rejection of claim 12.

As per claim 14, DPA discloses an apparatus for processing data (page 2 lines 19-21). All further limitations have been addressed in the above rejection of claim 1.

As per claims 15-17 and 20, the above rejection of claim 14 is incorporated. All further limitations have been addressed in the above rejections of claims 2-4 and 7, respectively.

8. Claims 5 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of DPA and Dale as applied to claim 1 above, and further in view of prior art of record U.S. Patent 5,555,392 to Chaput et al. (hereinafter referred to as "Chaput").

As per claim 5, the combination of DPA and Dale does not disclose *the apparatus as claimed in claim 1, wherein said data place holder includes data identifying how many outstanding late data values are awaited at that time.*

However, in an analogous environment, Chaput teaches the use of a field for counting the number of outstanding load misses (column 3 lines 35-36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Chaput's load miss field with the combination of DPA and Westcott's tracing mechanism. One of ordinary skill would have been motivated to track the status of pending load operations.

As per claim 18, the above rejection of claim 14 is incorporated. All further limitations have been addressed in the above rejection of claim 5.

9. Claims 6 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of DPA and Dale as applied to claims 1 and 14, respectively above, and further in view of prior art of record Chaput, and further in view of U.S. Patent 6,009,270 to Mann (hereinafter referred to as "Mann").

As per claim 6, the rejection of claims 1 and 5 are incorporated. DPA and Dale do not expressly disclose *the apparatus as claimed in claim 1, wherein said stream of trace data includes periodic synchronising data, said synchronising data including data identifying how many outstanding late data values are awaited at that time.*

However, in an analogous environment, Chaput teaches the use of a field for counting the number of outstanding load misses (column 3 lines 35-36). Further Mann teaches input of synchronization information into a data trace (column 2 lines 60-64).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Mann's synchronization stream with Chaput's outstanding load miss count with DPA and Dale's tracing circuit. One of ordinary skill would have been motivated to provide synchronization information to a tracing circuit to allow proper trace collection.

As per claim 19, the above rejection of claim 14 is incorporated. All further limitations have been addressed in the above rejection of claim 6.

10. Claims 8-10 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of DPA and Dale as applied to claims 7 and 20, respectively above, in view of prior art of record European Patent Application Publication 0 465 765 A2, "Instruction Sampling Instrumentation" by Westcott and White (hereinafter referred to as "Westcott").

As per claim 8, the above rejection of claim 7 is incorporated. DPA does not expressly disclose *wherein said tracing circuit is responsive to an exact match signal such that a trigger condition associated with a data value for which a data miss occurs is either:*

(i) not triggered until said data value is accessed and found to meet said trigger condition; or

(ii) triggered upon said data miss upon an assumption that said data value when accessed will meet said trigger condition.

However, in an analogous environment, Westcott teaches using a sample pulse signal to indicate a match reactive to a trigger condition associated with a data value (See column 6 lines 7-15 and 26-31).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Westcott's trigger with DPA's tracing circuit. One of ordinary skill would have been motivated to collect only that data which is of particular interest and which meets a selected requirement.

As per claim 9, the above rejection of claim 8 is incorporated. DPA does not expressly disclose *the apparatus as claimed in claim 8, wherein said exact match signal is user configurable.*

However, in an analogous environment, Westcott teaches user selected trigger conditions (column 6 lines 7-11).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Westcott's user selected trigger conditions with DPA's trigger circuit. One of ordinary skill would have been motivated to collect only that data which is of particular interest.

As per claim 10, the above rejection of claim 8 is incorporated. DPA does not expressly disclose *the apparatus as claimed in claim 8, wherein said exact match signal is set under hardware control depending upon a use of said trigger condition.*

However, in an analogous environment, Westcott teaches event selection (match signal) based on a trigger condition (column 6 lines 45-47).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Westcott's hardware event selection with DPA trigger circuit. One of ordinary skill would have been motivated to provide an automatic signal for triggering.

As per claims 21-23, the above rejection of claim 20 is incorporated. All further limitations have been addressed in the above rejections of claims 8-10, respectively.

11. Claims 11 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of DPA, Dale and Westcott as applied to claim 8 above, and further in view of prior art of record U.S. Patent 5,978,742 to Pickerd (hereinafter referred to as "Pickerd").

As per claim 11, the above rejection of claim 8 is incorporated. DPA does not expressly disclose: *the apparatus as claimed in claim 8, wherein said exact match signal has different values in different parts of said tracing circuit to provide two behaviors simultaneously.*

However, in an analogous environment, Pickerd teaches a circuit providing two trigger behaviors simultaneously (column 9 lines 36-41). All further limitations have been addressed in the above rejection of claim 8.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Pickerd's simultaneous trigger events and Westcott's behaviors with DPA's tracing circuit. One of ordinary skill in the art would be motivated to collect information relating to multiple trigger events to enable further customization.

As per claim 24, the above rejection of claim 21 is incorporated. All further limitations have been addressed in the above rejection of claim 11.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent 5659785 to Pechanek et al. teaches that data placeholders can be used in an instruction stream to hold a place for later subsitution of data. See column 5 line 42 – column 6 line 4.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to J. Derek Rutten whose telephone number is (571) 272-3703. The examiner can normally be reached on T-F 6:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jdr

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PRIMARY EXAMINER

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